Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-7. (Cancelled)

Claim 8. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 wherein an impedance of the first impedance termination circuit decreases by about 1/2 in response to the first bit shift signal, and the impedance of the first impedance termination circuit increases by about 2 in response to the second bit shift signal.

Claim 9. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 wherein the first impedance termination circuit includes five transistors coupled in parallel, the digital encoder circuit generates five digital signals, and the first multiplexers include five multiplexers.

Claim 10. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 wherein the first multiplexers receive n digital signals from the digital encoder circuit and pass each of the n digital signals from the digital encoder circuit to the first transistors without bit shifting the n digital signals in response to a bypass signal.

Claim 11. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 further comprising:

a second on-chip transistor coupled to the off-chip resistor; and

an analog-to-digital converter coupled to the first transistor and generating the analog signal.

Claim 12. (Currently amended) ~~The integrated circuit as defined in claim 5~~ An integrated circuit comprising:

a digital encoder circuit coupled to receive an analog signal indicative of an impedance of an off-chip resistor, the digital encoder circuit generating a plurality of digital signals;

a first bit shifter circuit comprising first multiplexers that receive the digital signals, wherein the first multiplexers shift the digital signals to the left in response to a first bit shift signal and to the right in response to a second bit shift signal; and

a first impedance termination circuit comprising first transistors coupled in parallel and that are each coupled to receive an output signal of one of the first multiplexers, each of the first transistors being coupled to a first pin of the integrated circuit,

wherein the first multiplexers shift the digital signals to the left by two bits in response to a third bit shift signal and to the right by two bits in response to a fourth bit shift signal.

Claim 13. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 further comprising:

logic array blocks, each including a plurality of logic elements that are configurable to implement logic functions; and

a programmable interconnect structure connecting the logic array blocks.

Claim 14. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 wherein the first impedance termination circuit is coupled to provide parallel termination impedance to the first pin.

Claim 15. (Currently amended) The integrated circuit as defined in claim ~~5~~ 12 wherein the first impedance termination circuit is coupled to provide series termination impedance to the first pin.

Claims 16-18. (Cancelled)

Claim 19. (Currently amended) The method according to claim ~~16~~ 21 further comprising:

shifting the digital signals by at least one bit to generate second bit shifted signals; and

setting a total impedance of second transistors using the second bit shifted signals, the second transistors being coupled in parallel, each of the second transistors being coupled to a second pin on the integrated circuit and to one of the second bit shifted signals.

Claim 20. (Cancelled)

Claim 21. (Currently amended) ~~The method according to claim 16~~ A method for providing termination impedance to a pin on an integrated circuit, the method comprising

generating digital signals in response to a signal indicative of an impedance of an off-chip resistor;

shifting the digital signals by at least one bit to generate bit shifted signals; and

setting a total impedance of first transistors using the bit shifted signals, the first transistors being coupled in parallel and to a first pin on the integrated circuit, each of the first transistors being coupled to receive one of the bit shifted signals,

wherein, the shifting of the digital signals includes passing all of the digital signals through multiplexers to generate the bit shifted signals, and

wherein shifting the digital signals by at least one bit to generate bit shifted signals further comprises:

shifting the digital signals by two bits to generate the bit shifted signals.

Claim 22. (Cancelled)

Claim 23. (Original) The method according to claim 19 wherein the first transistors are coupled to provide parallel termination impedance to the first pin; and the second transistors are coupled to provide series termination impedance to the second pin.

Claim 24. (Currently amended) The method according to claim ~~16~~ 21further comprising:

generating the signal indicative of the impedance of the off-chip resistor using an analog-to-digital converter circuit coupled to the off-chip resistors and an on-chip transistor.

Claim 25. (New) An integrated circuit comprising:

a first pin coupled to connect to a resistor that is external to the integrated circuit;

a first current source biased by a bias voltage and coupled to the first pin;

an analog-to-digital converter coupled to the first pin; and

a plurality of transistors forming a termination impedance, each coupled to one of a plurality of outputs of the analog-to-digital converter.

Claim 26. (New) The integrated circuit of claim 25 wherein the bias voltage compensates for changes in processing, supply voltage, and temperature.

Claim 27. (New) The integrated circuit of claim 25 further comprising a logic circuit coupled between the analog-to-digital converter and the plurality of transistors.

Claim 28. (New) The integrated circuit of claim 27 wherein the logic circuit converts outputs of the analog-to-digital converter to binarily-weighted output signals.

Claim 29. (New) The integrated circuit of claim 27 wherein the logic circuit output signals are binarily weighted.

Claim 30. (New) The integrated circuit of claim 27 wherein the logic circuit can right shift the output signals before providing them to the output transistors, can left shift the output signals before providing them to the output transistors, or not shift the output signals before providing them to the plurality of transistors.

Claim 31. (New) An integrated circuit comprising:

a first on-chip termination impedance circuit comprising a first plurality of parallel transistors coupled to a first pad;

a first control circuit coupled to adjust the termination impedance of the first on-chip termination impedance circuit by providing a first plurality of control signals to the first on-chip impedance circuit, wherein the first plurality of control signals can be right shifted, left shifted, or not shifted before being provided to the first on-chip termination impedance circuit;

a second on-chip termination impedance circuit comprising a second plurality of parallel transistors coupled to a second pad; and

a second control circuit coupled to adjust the termination impedance of the second on-chip termination impedance circuit by providing a second plurality of control signals to the second on-chip impedance circuit, wherein the second plurality of control signals can be right shifted, left shifted, or not shifted before being provided to the second on-chip termination impedance circuit.

Claim 32. (New) The integrated circuit of claim 31 wherein the first on-chip termination impedance circuit comprises a plurality of transistors, each having a drain coupled to the first pad, and the second on-chip termination impedance comprises a plurality of transistors, each having a drain coupled to the second pad.

Claim 33. (New) The integrated circuit of claim 31 wherein the first on-chip termination impedance circuit is coupled to a source of an output driver transistor, wherein a drain of the output driver transistor is coupled to the first pad.

Claim 34. (New) The integrated circuit of claim 31 wherein the first plurality of control signals are right shifted, left shifted, or not shifted, independently of whether the second plurality of control signals are right shifted, left shifted, or not shifted.